REMARKS

Claims 1 and 2 were rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 1 was rejected under 35 U.S.C. 112, second paragraph, as being indefinite. Claim 1 is amended in response to the examiners rejection. The condition that a current flowing through the source/drain terminals of the NMOS pass transistor is greater than a current flowing through the source/drain terminals of the PMOS drive transistor for the same voltages applied between the gate and source/drain terminals of the PMOS drive transistor and the gate and source/drain terminals of the NMOS pass transistor has been added to a description of the transistors. This should clarify the fact that this is a characteristic of the transistors used to form the memory cell rather than memory cell operation.

Claims 1 and 2 were rejected under 35 U.S.C. 102(a) as being anticipated by Portacci.

In the Portacci patent (6,172,901) lines 23-30 described by the examiner refer to Figure 9 and not Figure 1. Therefore the description is not relevant to Figure 1. Furthermore and more importantly the text reads, "When using PMOS transistors for the pass transistors 226, 236, the designer must be aware that the reading current will be less than if NMOS transistors are used, such as in the memory cell 110." Clearly this is comparing PMOS and NMOS pass transistors. The circuit of the instant invention describes PMOS drive transistors and NMOS pass transistors. It is clear therefore that the Portacci patent is not a valid 102(a) reference.

In light of the above, it is respectfully submitted that the present application is in condition for allowance, and notice to that effect is respectfully requested.

While it is believed that the instant amendment places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with Markings to Show Changes Made."**

To the extent necessary, Applicants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,

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Version with Markings to Show Changes Made

1(Amended). A memory cell, comprising:

providing a PMOS drive transistor with a gate terminal, a first source/drain terminal, and a second source/drain terminal;

providing a NMOS pass transistor with a gate terminal, a first source/drain terminal and a second source/drain terminal wherein a current flowing through the source/drain terminals of the NMOS pass transistor is greater than a current flowing through the source/drain terminals of the PMOS drive transistor for the same voltages applied between the gate and source/drain terminals of the PMOS drive transistor and the gate and source/drain terminals of the NMOS pass transistor ;

connecting said first source/drain terminal of said NMOS pass transistor to a bitline;

connecting said second source/drain terminal of said NMOS pass transistor to a first storage node;

connecting said gate terminal of said NMOS pass transistor to a wordline;

connecting said first source/drain terminal of said PMOS drive transistor to a supply voltage;

connecting said second source/drain terminal of said PMOS drive transistor to said first storage node; and

connecting said gate terminal of said PMOS drive transistor to a second storage node[; and] .

[wherein a current flowing through the source/drain terminals of the NMOS pass transistor is greater than a current flowing through the source/drain terminals of the PMOS drive transistor for the same voltages applied between the gate and source/drain terminals of the PMOS drive transistor and the gate and source/drain terminals of the NMOS pass transistor.]